IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jeffery W. Janzen et al.		§	Confirmation No.: 9165
		§	
		§	Group Art Unit: 2116
Serial No.:	10/816, 239	§	
		§	Examiner: Rahman, Fahmida
Filed:	April 1, 2004	§	
		§	
For:	Memory Modules Having Accurate Operating Current Values of Stored Thereon and Methods for Fabricating And Implementing Such Devices	§ § § §	Atty. Docket: MICS:0103/MAN/ROG 02-1327

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February 11, 2008	**/Robert A. Manware/**
Date	Robert A. Manware

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal electronically filed on December 10, 2007.

1. REAL PARTY IN INTEREST

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application by virtue of the Assignment to Micron Technology, Inc., recorded at reel 015181, frame 0692, and dated April 1, 2004. Accordingly, Micron Technology, Inc., will be directly affected by the Board's decision in the pending appeal.

2. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. STATUS OF CLAIMS

Claims 1-32 are currently pending, are currently under final rejection and, thus, are the subject of this Appeal.

4. STATUS OF AMENDMENTS

As there were no amendments made to the claims after the Final Office Action issued, there are no outstanding amendments to be considered by the Board.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates generally to memory subsystems. Specifically, the present invention relates to programming a memory module with accurate operating current values that are unique to specific memory devices rather than a general characterization of devices of a particular type. *See* Application, page 1, lines 8-10; page 12, lines 15-18. As discussed in the present application, a typical computer system may include a memory module, such as an In-line Memory Module (IMM) or Dual In-line Memory Module (DIMM), containing individual memory devices packaged together on a circuit board. Application, page 9, line 20 – page 10, line 3; Fig. 3. During operation of the computer, the writing and reading of data to and from a memory device causes the memory device to draw current and increase in temperature.

Application, page 3, lines 1-6. The more frequently memory data is accessed, the more current the memory device draws and the hotter the device becomes, making it more likely that the device will fail due to overheating. Application, page 11, lines 11-13. To solve this problem, computers are often programmed to limit the memory clock speed as a way of ensuring that the device will remain below a certain specified operating current and, therefore, within a safe operating temperature. Application, page 3, lines 12-15. To facilitate this process, the maximum current that the memory device can handle is typically programmed into the memory module. *See* Application, page 10, lines 22-24. This current value, known as the "operating current," is typically programmed into a Serial Presence Detect (SPD), which is a non-volatile memory device such as an Electrically Erasable Programmable Read-only Memory (EEPROM) used to store various information relating to the memory devices within the memory module. *Id.* The operating current is read from the SPD by the computer system, which is programmed to ensure that the actual current in the memory device does not exceed the specified operating current. Application, page 10, lines 18-21; page 11, lines 14-17.

In the prior art, memory modules are typically programmed with operating currents that are device-type specific. Application, page 11, lines 19-22. For example, operating currents are generally derived from data sheets which provide Industry Standard operating current values used for specific types of memory devices. Application, page 11, lines 5-7. The problem with this approach is that the Industry Standard operating current for a particular device represents the worst-case (i.e. minimum) operating current that the device must be able to handle without overheating; however, depending on the quality of the actual manufactured device, the device may be capable of maintaining a safe temperature at a much higher operating current than is specified in the data sheet. *See* Application, page 11, line 22 – page 12, line 5. According to the present invention, therefore, actual operating current values are measured for specific individual memory devices, and the memory modules are then programmed to operate at the higher operating currents that are unique to a particular device rather than the Industry Standard operating current values specified for a particular

type of device. *See* Application, page 12, lines 5-7. In this way, the memory devices may be driven at a higher operating current while still ensuring that the memory device will not overheat. *See Id.*

Aspects of the present invention also include storing operating current values that are unique to a particular manufacturing lot rather than a specific individual memory device. Application, page 13, lines 5-8. It will be appreciated by those of ordinary skill in the art that a manufacturing lot refers to a group of devices that are manufactured using the same production line setup. The devices within a manufacturing lot will, therefore, tend to have similar operating characteristics. Accordingly, aspects of the present invention involve measuring the operating current for individual memory devices within a particular manufacturing lot and computing an average operating current for memory devices within this lot. *See* Application, page 12, lines 19-21. The memory module is then programmed with this operating current, which is unique to the manufacturing lot. *See* Application, page 13, lines 5-8.

The Application contains seven independent claims, namely, claims 1, 7, 13, 17, 21, 25 and 29, all of which are the subject of this Appeal. The subject matter of these claims is summarized below.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the below cited locations of the specification and drawings. By way of example an embodiment in accordance with claim 1 provides a method of configuring a system. *See* Application, Fig. 5. The method of configuring a system comprises reading operating current values from a non-volatile memory device on a memory module (e.g., 54). *See* Application, page 14, lines 7-9; Fig. 5. The memory module comprises a plurality of volatile memory devices (e.g., 42A-H). *See* Application, page 12, lines 9-13; Fig. 3. The operating current values comprise operating currents uniquely corresponding to a lot in which the volatile memory devices were manufactured (e.g., 48). *See* Application, page 12, lines 19-22; Fig. 4. The

method further comprises configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module (e.g, 56, 58). *See* Application, page 14, lines 7-17; Fig. 5.

With regard to the aspect of the invention set forth in independent claim 7, discussions of the recited features of claim 7 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 7 provides a method of configuring a system. *See* Application, Fig. 5. The method of configuring a system comprises reading operating current values from a non-volatile memory device on a memory module (e.g., 54). *See* Application, page 14, lines 7-9; Fig. 5. The memory module comprises a plurality of volatile memory devices (e.g., 42A-H). *See* Application, page 12, lines 9-13; Fig. 3. The operating current values comprise operating currents uniquely corresponding to each of the plurality of memory devices. *See* Application, page 13, lines 1-3. The method further comprises configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module (e.g., 56, 58). *See* Application, page 14, lines 7-17; Fig. 5.

With regard to the aspect of the invention set forth in independent claim 13, discussions of the recited features of claim 13 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 13 provides a method of manufacturing a memory module. *See* Application, Fig. 4. The method of manufacturing a memory module comprises measuring operating current values in each of a plurality of volatile memory devices (e.g., 46). *See* Application, page 12, lines 9-13; Fig. 4. The method further comprises storing each of the operating current values corresponding to each of the plurality of volatile memory devices in a non-volatile memory device (e.g., 50). *See* Application, page 13, lines 5-8; Fig. 4. The method further comprises forming a memory module comprising each of the plurality of volatile memory devices and the non-volatile memory device (e.g., 52). *See* Application, page 13, lines 8-12; Fig. 4.

With regard to the aspect of the invention set forth in independent claim 17, discussions of the recited features of claim 17 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 17 provides a method of manufacturing a memory module. *See* Application, Fig. 4. The method of manufacturing a memory module comprises measuring operating current values in each of a plurality of volatile memory devices (e.g., 46). *See* Application, page 12, lines 9-13; Fig. 4. The plurality of volatile memory devices correspond to a single manufacturing lot (e.g., 48). *See* Application, page 12, lines 19-21; Fig. 4. The method further comprises calculating average operating current values for the manufacturing lot (e.g., 48). *See* Application, page 12, lines 19-21; Fig. 4. The method further comprises storing the average operating current values in a non-volatile memory device (e.g., 50). *See* Application, page 13, lines 5-8; Fig. 4. The method further comprises forming a memory module comprising each of the plurality of volatile memory devices and the non-volatile memory device (e.g., 52). *See* Application, page 13, lines 8-12; Fig. 4.

With regard to the aspect of the invention set forth in independent claim 21, discussions of the recited features of claim 21 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 21 provides a memory module (e.g., 34). *See* Application, page 9, line 20; Fig. 3. The memory module comprises a plurality of volatile memory devices (e.g., 42A-H). *See* Application, page 10, lines 1-3; Fig. 3. The memory module further comprises a non-volatile memory device having operating current values uniquely corresponding to a lot in which the plurality of volatile memory devices were manufactured stored thereon (e.g., 44). *See* Application, page 10, lines 22-24; page 13, lines 5-7; Fig. 3.

With regard to the aspect of the invention set forth in independent claim 25, discussions of the recited features of claim 25 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 21 provides a memory module (e.g., 34). *See* Application, page 9,

line 20; Fig. 3. The memory module comprises a plurality of volatile memory devices (e.g., 42A-H). *See* Application, page 10, lines 1-3; Fig. 3. The memory module further comprises a non-volatile memory device having operating current values uniquely corresponding to each of the plurality of volatile memory devices stored thereon (e.g., 44). *See* Application, page 10, lines 22-24; page 13, lines 5-7; Fig. 3.

With regard to the aspect of the invention set forth in independent claim 29, discussions of the recited features of claim 29 can be found at least in the below cited locations of the specification and drawings. By way of example, an embodiment in accordance with claim 29 provides a computer system (e.g., 10). *See* Application, Fig. 1. The computer system comprises a processor (e.g., 12). *See* Application, page 6, lines 5-7; Fig. 1. The computer system further comprises a memory module coupled to the processor (e.g., 12). *See* Application, page 7, lines 9-19. The memory module comprises a plurality of volatile memory devices (e.g., 26). *See* Application, page 7, lines 11-13; Fig. 1. The memory module further comprises a non-volatile memory device having operating current values uniquely corresponding to each of the plurality of volatile memory devices stored thereon (e.g., 28). *See* Application, page 7, lines 19; page 12, lines 15-17; Fig. 1.

6. <u>GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL</u>

<u>First Ground of Rejection for Review on Appeal</u>:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1-5 and 21-24 under 35 U.S.C. §103(a) as being unpatentable over Trick, U.S. Patent No. 5,995,405 (hereinafter referred to as "Trick"), in view of Abrahams et al., U.S. Patent Application Publication 2004/0078454 (hereinafter referred to as "Abrahams"), further in view of Nerl, U.S. Patent Application Publication 2002/0016897 (hereinafter referred to as "Nerl").

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 7-11 and 25-32 under U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams.

Third Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's third ground of rejection in which the Examiner rejected claim 6 under U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams, in view of Nerl, and further in view of Wu, U.S. Patent No. 7,064,994 (hereinafter referred to as "Wu").

Fourth Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's fourth ground of rejection in which the Examiner rejected claim 12 under U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams, further in view of the Wu.

Fifth Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's fifth ground of rejection in which the Examiner rejected claims 13-20 under U.S.C. §103(a) as being unpatentable over Abrahams, in view of Nerl.

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Section 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-32 are currently in condition for allowance.

Throughout Appellants' specification, including the claims, and throughout the prosecution history of the present application, Appellants have repeatedly distinguished

between operating current values that are: 1) device-type specific; 2) manufacturing lot specific; and 3) device specific. Application, page 11, lines 19-24; page 12 lines 5-7; page 12, line 13 – page 13, line 4; Response to Office Action mailed March 3, 2007, page 12; Response to Final Office Action mailed September 10, 2007, page 11. In accordance with embodiments recited in various independent claims, embodiments of the invention are directed to the utilization of lot specific or device specific operating current values of volatile memory devices. By measuring each device and storing values associated with each specific device or storing values associated with a particular lot, rather than relying on device-type characterizations, as in the prior art, the operating current values for a specific device or operating current values corresponding to a specific manufacturing lot in which a particular device was manufactured, operation of the devices may be optimized. Application, page 12, lines 5-7.

Appellants stress that this utilization of *device specific* or *manufacturing lot specific* operating current values, which are based upon actual values measured for those specific devices being employed, is *not* taught by the cited references. Indeed, Abrahams, Nerl and Trick each disclose using device-type specific operating current values. Indeed, this is completely consistent with the Appellants' description of the prior art and in stark contrast to each of Appellants' claims.

With regard to Trick, Appellants have continued to argue that Trick does not teach storing device-specific or lot-specific operating current values. The Examiner disagrees, stating in the final office action, mailed September 10, 2007, (hereinafter referred to as "Final Office Action") that "Trick indicates that the other 128 bytes are reserved for either manufacturer or purchaser of IMM (lines 49-53 of column 1). Final Office Action, page 16. Therefore, the information/values stored thereon uniquely corresponds to the lot of IMM." Appellants respectfully disagree. Although Trick does teach that "128 bytes are usually reserved for use by either the manufacturer or the purchaser of the IMM," it does not follow that the information stored thereon uniquely corresponds to the individual memory devices on the IMM. Nor does it follow that the

information stored thereon uniquely corresponds to a manufacturing lot of memory devices. Moreover, Trick in no way suggests the storage of *operating currents* specific to the individual memory devices on the IMM. In fact, Trick would appear to teach away from the present invention, because in the same passage cited by the Examiner, Trick expressly teaches the use of Industry Standard information (Trick, col. 1, lines 45-47), whereas the present invention makes Industry Standard information irrelevant insofar as it pertains to operating current.

What Trick *does* teach is the reservation of *empty memory space* on the EEPROM of an IMM. *Id.*, col. 1, lines 43-50. If the present rejections are valid, then it is conceivable that any novel use of computer memory could be anticipated by a reference that recites unused computer memory; the argument being that the unused memory space could have been used in the way that is being claimed. This is clearly erroneous.

The Examiner responded to the above argument, regarding Trick, by stating that "Trick teaches reserved space for each IMM. Any information stored there is specific to that IMM, or lot, since that reserved space is programmed by the purchaser or manufacturer." Advisory Action, page 2. Based on the above argument, it would appear that the Examiner's rejection is based on a misconception of the term "lot" as it is used in the Application. Specifically, the Examiner appears to be interpreting the lot to be the IMM itself. The term "lot" does not, however, refer to an individual IMM, a manufacturing lot of IMMs, or a group or memory devices on an IMM. In fact, Appellants have, throughout prosecution, maintained that the term "lot," as consistently used in the specification of the present invention refers to a manufacturing lot of memory devices, some of which may be installed on a particular IMM.

In response to the Appellants' attempt to clarify the meaning of the term "manufacturing lot," the Examiner has stated that the terms "manufacturing lot" and "lot" were not defined in the specification, implying that the Appellants' arguments regarding these terms are, therefore, irrelevant. Advisory Action, page 2. However, the

specification makes clear the meaning intended by the terms "lot" and "manufacturing lot." For example, the specification first describes a memory module, or IMM, as "includ[ing] a plurality of volatile memory devices 42A-42H, such as dynamic random access memory devices (DRAMs), which may be used for storing information." Application, page 10, lines 13-15. The specification then states that "[b]y setting operating current thresholds in the system 10, based on the operating current values stored on the non-volatile memory device 44 and corresponding uniquely to the memory devices 42A-42H *or to the lot from which the memory devices 42A-42H were manufactured*, access rates to memory devices 42A-42H can generally be increased." Application, page 15, lines 7-11 (emphasis added). Therefore, a person of ordinary skill in the art would recognize that the term "manufacturing lot" refers to a manufacturing lot of memory devices, some of which are installed on a particular IMM.

Regarding Abrahams, Appellants have continued to argue that Abrahams also does not teach storing device specific or lot specific operating current values. The Examiner disagrees, stating in the office action that "Abrahams mention about reading operating current values from non-volatile memory of the component. Therefore, with the teaching of Abrahams, the values stored in non-volatile memory of Trick, which uniquely corresponds to a lot where volatile memory devices were manufactured, can be operating current values." Final Office Action, page 17. Appellants respectfully disagree. The Examiner's argument fails to acknowledge the difference between Industry Standard operating current values, which are only device-*type* specific, and the operating current values used in the present invention which are *device* specific or *manufacturing lot* specific (i.e., uniquely corresponding to the specific device being employed or uniquely corresponding to the lot in which the specific device was manufactured). While Abrahams does teach the use of operating current values, Abrahams does not teach the use of *device-specific* operating current values, i.e., operating current values that have been measured for and pertain to only one particular memory device.

The Examiner also stated that he could not find support in Abrahams for

Appellants' contention that the operating currents of Abrahams are nothing more than Industry Standard operating currents. However, Abrahams states that "[t]he operational parameters may be specific to each *type* of component." Abrahams, paragraph 23; *see also*, *id.* paragraph 24. This lends support to Appellants' argument that the operating current values used in Abrahams are Industry Standard values because the Industry Standard values are typically used to characterize *types* of components (e.g., DRAM). Even if the operational parameters of Abraham's can be construed to be something other than Industry Standard values, the important point is that they are device-*type* specific.

Even more importantly, nothing in Abrahams affirmatively suggests that the operational parameters are *device* specific as opposed to *device-type* specific. The Examiner agrees that "Abrahams does not mention how the operating values are determined," but the Examiner then states that Appellants' arguments "do not preclude the values to be measured." Final Office Action, page 18. Appellants object to this line of reasoning because although an invention can be obvious over subject matter that is disclosed in prior art, it cannot be obvious over subject matter that is not precluded because it is never mentioned at all. By stating that Abrahams does not preclude the operating values to be measured, the Examiner has effectively read subject matter into Abrahams that is not there.

Additionally, in response to the Appellants' arguments that Trick and Abrahams teach only the use of device-type specific, or Industry Standard operating currents, the Examiner has stated that "such arguments are irrelevant, because claims only require currents to be unique to lot, no matter how it is unique to lot. Here currents are unique to the lot, as number of components present in the lot defines the currents values stored in the non-volatile memory." Advisory Action, page 2. The Appellants believe that this argument is flawed in at least two ways.

First, as discussed above, the Examiner appears to be equating the "lot" with the IMM itself, when in fact the "lot" pertains to the manufacturing lot in which the memory

devices were manufactured. The claims of the present invention, therefore, recite operating currents that are unique to the manufacturing lot of memory devices, not to the IMM, as the Examiner seems to believe.

Secondly, independent claims 7, 13 and 29 do not recite a manufacturing lot at all. Rather, claims 7, 13, and 29 recite the use of operating currents that are unique to particular memory devices being employed in the memory module. As stated above, this stands in stark contrast to the prior art, in which the operating currents stored on an IMM are only device-type specific, i.e. Industry Standard values. To say that such arguments are irrelevant is to ignore the central thrust of the entire application, including the claims, which has clearly stated that the novelty of certain embodiments of the present invention lie in the use of device specific operating currents as opposed to Industry Standard or device-type specific operating currents. *See*, *e.g.*, Application, page 4, lines 7-14; page 11, line 19 – page 12, line 7; page 12, line 13 – page 13, line 1.

Appellants also note that the Examiner rejected claims 1-32 on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-12 U.S. Pat. No. 7,035,159, and provisionally rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-30 of copending Application No. 10/816,241. This issue is not on appeal before the Board. Although Appellants do not necessarily agree with the Examiner's assertion, Appellants may be amenable to filing a terminal disclaimer upon allowance of the claims in the present application. Any such filing will depend on the prosecution, and state of claims in the present application at the time of allowance. Accordingly, Appellants respectfully request that the Board hold in abeyance the double-patenting rejection until the present claims are determined to be allowable.

A. **Ground of Rejection No. 1:**

The Examiner rejected claims 1-5 and 21-24 under 35 U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams, and further in view of Nerl. Appellants respectfully traverse this rejection.

1. **Judicial precedent has clearly established a legal standard for a *prima facie* obviousness rejection.**

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). In establishing a *prima facie* case for obviousness, it is often necessary "to look to interrelated teachings of multiple patents, the effects of demands known to the design community or present in the market place; and the background knowledge possessed by a person having ordinary skill in the art." *KSR Int'l Co. v. Teleflex, Inc.* No. 04-1350, slip op. at 14 (U.S. April 30, 2007). Indeed, "the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the subject matter is determined." *Id.* at 2 (quoting *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). This analysis should be made explicit. *Id.* at 14 (citing *In re Khan*, 441 F.3d 977, 988 (Fed. Cir. 2006)) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness").

Additionally, a claim having several elements is *not* proved obvious merely by demonstrating that each of its elements was known in the prior art. *Id.* As such, the obviousness inquiry does not hinge on demonstrating that elements were known in the art. Rather, the obviousness inquiry focuses on whether the claimed subject matter would have been obvious to persons having ordinary skill in the art in view of the demands and practices of the design community at the time of filing of the application. *See id.*

2. **<u>The Examiner's rejection of claims 1-5 and 21-24 is improper because the cited references, alone or in combination, lack features recited in independent claims 1 and 21 and claims depending therefrom.</u>**

Computer device manufacturers design memory devices to operate within a predetermined temperature range. Application, page 2, lines 19-20. Given that the memory devices in a computer system employ electric current to perform their intended functions, the amount of heat in the device is a function of the flow of current through the device. Application, page 3, lines 4-7. Accordingly, memory devices are typically accompanied by data sheets specifying operating currents for the devices in various modes and conditions. Application, page 3, lines 21-23. These data sheets correspond to a given type of memory chip and represent the worst case scenario for that particular type of device. Application, page 4, lines 7-9. Any given memory device can often operate at currents 15-40% outside of the data sheet values. Application, page 3, lines 10-12. Therefore, by implementing the data sheet values, the full extent of the device's capabilities are not being exploited. Application, page 3, lines 12-14.

Accordingly, independent claims 1 and 21 of the present application recite the utilization of "operating currents *uniquely* corresponding to a *lot* in which the [plurality of] volatile memory devices were manufactured," rather than utilization of the general device-type specific operating currents that are typically listed on data sheets. (Emphasis added.) By implementing the lot-specific operating current values, claims 1 and 21 provide a more accurate technique than the typical data sheet-based methods which employ device-type specific data. Application, page 12, line 24 – page 13, line 1. Consequently, the method of claim 1 and the memory module of claim 21 result in a more efficient use of the specific memory device's capabilities.

Appellants respectfully submit that neither Trick, Abrahams, nor Nerl, alone or in combination, disclose each and every feature of independent claims 1 and 21. Specifically, none of the aforementioned references teaches utilizing operating currents

uniquely corresponding to a *lot* in which the memory devices were manufactured, as recited in claims 1 and 21.

Regarding Trick, the Examiner asserted that Trick teaches utilizing operating parameters uniquely corresponding to a lot in which the volatile memory devices were manufactured. Final Office Action, page 4. Specifically, the Examiner asserted that the electrically erasable programmable ROM (EEPROM) disclosed in Trick is associated with In-line Memory Modules (IMMs) and, therefore, identifies the lot of memory devices. *Id.* Appellants respectfully disagree and respectfully submit that Trick does not teach operating parameters uniquely corresponding to a lot in which the volatile memory devices were manufactured, as asserted by the Examiner.

Rather, Trick discloses a mechanism for adapting an IMM so that it may be configured to accommodate a standard EEPROM or a "daisy chain" EEPROM. Trick, col. 2, lines 21-25. Trick is not concerned with improving the accuracy of determining operating parameters of memory devices, specifically the operating current, as in the present application. Indeed, Trick discloses in general terms the functions of the EEPROM, but does not discuss the operating parameters of the IMM. Trick, col. 1, lines 43-56. To the extent that Trick discloses that configuration information is stored on the EEPROM, Trick fails to teach that the configuration information is lot-specific configuration information. *See id.*, col. 1, lines 31-34. Therefore, Trick does not disclose the utilization of "operating currents uniquely corresponding to a lot in which the [plurality of] volatile memory devices were manufactured," as recited by independent claims 1 and 21.

Further, Appellants assert that the Examiner's attempt to remedy the deficiencies of Trick by citing Abrahams is insufficient. The Examiner merely relied on Abrahams for its alleged disclosure of reading operating current values from a non-volatile memory device on a memory module. Final Office Action, page 5. To the extent Abrahams may disclose the reading of operating current values, nowhere does Abrahams teach or

suggest that those operating current values "uniquely correspond[] to a lot in which the volatile memory devices were manufactured," as recited in independent claims 1 and 21. For example, Abrahams provides that "[t]he operational parameters may be *specific to each type of component*. For example, disk drives may have different operational parameters than array controllers." Abrahams, page 2, paragraph 23 (emphasis added). Therefore, the specification in Abrahams teaches utilizing parameters specific to a particular type of component and not lot-specific parameters. In fact, Abrahams is devoid of any mention of lot-specific parameters such as lot-specific current values. The inaccuracy and inefficiency associated with using values associated with a particular type of component is exactly the problem that implementation of the present invention is designed to eliminate. Therefore, Abrahams does not disclose the utilization of "operating currents uniquely corresponding to a lot in which the [plurality of] volatile memory devices were manufactured," as recited in claims 1 and 21.

Appellants further assert that Nerl fails to remedy the deficiencies of either Trick or Abrahams. Indeed, the Examiner merely referred to Nerl for its alleged teaching that it is well known in the art that a DIMM can be an FRU. Final Office Action, page 5. Accordingly, even if Nerl disclosed what is asserted by the Examiner, it does not remedy the deficiencies discussed above.

In view of the remarks set forth above, Appellants respectfully submit that independent claims 1 and 21 and their dependent claims are not rendered obvious by the cited combination. Accordingly, Appellants request withdrawal of the Examiner's rejection and the allowance of claims 1-5 and 21-24.

B. **Ground of Rejection No. 2:**

The Examiner rejected claims 7-11 and 25-32 under 35 U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams. Appellants respectfully traverse this rejection.

1. **The Examiner's rejection of claims 7-11 and 25-32 is improper because the cited references, alone or in combination, lack features recited in independent claims 7, 25 and 29 and claims depending therefrom.**

Independent claims 7, 25, and 29 of the present application recite the utilization of "operating currents uniquely corresponding to each of the plurality of memory devices," rather than utilization of the general device-type specific operating current currents that are typically listed on data sheets. By implementing the operating currents specific to each unique memory device, claims 7, 25, and 29 provide a more accurate technique than the typical data sheet-based methods. Application, page 12, lines 24 – page 13, line 1. Consequently, the method of claim 7, the memory module of claim 25, and the computer system of claim 29 result in a more efficient use of the specific memory device's capabilities.

Appellants respectfully submit that neither Trick nor Abrahams, alone or in combination, disclose each and every feature of independent claims 7, 25, and 29. Indeed, given that the operating currents specific to each memory device recited in independent claims 7, 25, and 29 offer the same advantages as the lot-specific values utilized in independent claims 1 and 21, Appellants rely on the remarks presented above to demonstrate that neither Trick nor Abrahams teach the utilization of operating currents *uniquely* corresponding to *each* of a plurality of memory devices. Accordingly, Appellants request withdrawal of the Examiner's rejection and allowance of claims 7-11 and 25-32.

C. **Ground of Rejection No. 3:**

The Examiner rejected claim 6 under 35 U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams, further in view of Nerl, and further in view of Wu. Appellants respectfully traverse this rejection.

1. **<u>The Examiner's rejection of claim 6 is improper because the cited references, alone or in combination, lack features recited in claim 6.</u>**

In the rejection of dependent claim 6, the Examiner asserted that Trick in view of Abrahams, in view of Nerl and further in view of Wu discloses all of the recited features. Appellants respectfully assert that the rejection is deficient because neither Nerl, nor Wu, alone or in hypothetical combination, remedy the deficiencies of Trick and Abrahams. That is that neither Nerl, nor Wu obviates the deficiencies of Trick and Abrahams discussed above with reference to independent claim 1. For at least this reason, Appellants submit that Trick, Abrahams, Nerl and Wu, alone or in combination, do not disclose each and every feature of dependent claim 6. Accordingly, Appellants respectfully request withdrawal of the rejection of claim 6 under 35 U.S.C. § 103.

D. **<u>Ground of Rejection No. 4</u>:**

The Examiner rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over Trick, in view of Abrahams, and further in view of Nerl. Appellants respectfully traverse this rejection.

1. **<u>The Examiner's rejection of claim 12 is improper because the cited references, alone or in combination, lack features recited in claim 12.</u>**

In the rejection of dependent claim 12, the Examiner asserted that Trick in view of Abrahams, and further in view of Wu discloses all of the recited features. Appellants respectfully assert that the rejection is deficient because Wu does not remedy the deficiencies of Trick and Abrahams. That is that Wu does not obviate the deficiencies of Trick and Abrahams discussed above with reference to independent claim 7. For at least this reason, Appellants submit that Trick, Abrahams, and Wu, alone or in combination, do not disclose each and every feature of dependent claim 12. Accordingly, Appellants respectfully request withdrawal of the rejection of claim 12 under 35 U.S.C. § 103.

E. **<u>Ground of Rejection No. 5</u>:**

The Examiner rejected claims 13-20 under 35 U.S.C. §103(a) as being unpatentable over Abrahams, and further in view of Nerl. Appellants respectfully traverse this rejection.

1. **<u>The Examiner's rejection of claims 13-20 is improper because the cited references, alone or in combination, lack features recited in independent claims 13 and 17 and claims depending therefrom.</u>**

<u>A. Claim 13</u>

In accordance with embodiments of the present techniques, memory devices may be individually tested such that device-specific operating current values uniquely corresponding to each memory device can be recorded and stored in a database. Application, page 13, lines 20-23. In one embodiment, the operating current values in the database may be used during fabrication of a memory module wherein the database is accessed during fabrication and a non-volatile memory device may be uniquely programmed in accordance with the specific operating current values for the particular memory devices on the memory module. Application, page 13, line 13 – page 14, line 4. After fabrication and programming of the non-volatile memory device, a memory module can be shipped for implementation in a system and operating current values may be accessed by the system from the non-volatile memory device such that the system can be configured to operate optimally within the capabilities of the particular memory devices. Application, page 14, lines 4-9.

Accordingly, claim 13 recites a method of manufacturing a memory module comprising, *inter alia*, "measuring operating current values in each of a plurality of volatile memory devices;" and "storing each of the operating current values corresponding to each of the volatile memory devices in a non-volatile memory device."

In the rejection of claim 13, the Examiner stated that Abrahams discloses "measuring operating current values in each of a plurality of memory devices (lines 13-

15 of page 1)." Final Office Action, page 13. The Examiner further stated that Abrahams discloses "storing each of the operating current values corresponding to each of the plurality of memory devices in a non-volatile memory device." *Id.* Appellants respectfully disagree with the Examiner's assertions regarding Abrahams.

Claim 13 recites measuring operating current values in each of a plurality of volatile memory devices and storing each of the operating current values in a non-volatile memory device. While Appellants agree that Abrahams does teach storing operational parameters in a non-volatile memory device, these operational parameters are specific to a type of component, such as those found on a component's data sheet. Abrahams, page 2, paragraph 22. The operational parameters that may be stored on the non-volatile memory device are not the operating current values that were measured for each of a plurality of volatile memory devices. Indeed, to the extent Abrahams discloses the measuring of operational parameters, Appellants respectfully submit that Abrahams discloses the measuring of the current operating conditions of the component. Abrahams, page 1, paragraph 11. The current operating conditions of the component then may be compared to the operational parameters for a type of component that may be stored in the non-volatile memory. *Id.* Accordingly, Abrahams does not disclose measuring operating current values in each of a plurality of memory devices and storing each of the operating current values in a non-volatile memory device.

Appellants further assert that Nerl fails to remedy the deficiencies of Abrahams. Indeed, the Examiner merely referred to Nerl for its alleged teaching that it is well known in the art that a DIMM can be an FRU. Final Office Action, page 13. Accordingly, even if Nerl disclosed what is asserted by the Examiner, it does not remedy the deficiencies discussed above.

In view of the remarks set forth above, Appellants respectfully submit that independent claim 13 and its dependent claims are not rendered obvious by the cited combination. Accordingly, Appellants request withdrawal of the Examiner's rejection

and allowance of claims 13-16.

B. Claim 17

Claim 17 recites, *inter alia*, "measuring operating current values in each of a plurality of volatile memory devices, wherein the plurality of volatile memory devices correspond to a single manufacturing lot; calculating average operating current values for the manufacturing lot;" and "storing the average operating current values in a non-volatile memory device."

As discussed above with respect to the rejection of claim 13, Abrahams does not disclose measuring operating current values in each of a plurality of volatile memory devices. Indeed, to the extent Abrahams discloses the measuring of operational parameters, Appellants respectfully submit that Abrahams discloses the measuring of the current operating conditions of the component. Abrahams, page 1, paragraph 11. Further, nowhere does Abrahams disclose that the operating current values are measured for a plurality of volatile memory devices that correspond to a single manufacturing lot. Accordingly, Abrahams does not disclose measuring operating current values in each of a plurality of volatile memory devices, wherein the plurality of memory devices correspond to a single manufacturing lot.

Moreover, in contrast to the present claims and as admitted by the Examiner, Abrahams also does not disclose "calculating *average* operating current values for the manufacturing lot" and "storing the *average* operating current values in a non-volatile memory device," as recited by independent claim 17. *See* Final Office Action, page 15 . Rather, the Examiner argues that "one of ordinary skill in the art would have been motivated to store average current corresponding to the lot in the non-volatile memory depending on his design choice." *Id.* Appellants respectfully disagree and submit that the Examiner has not demonstrated a "convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I.

1985). Indeed, as previously mentioned, Abrahams is devoid of any disclosure regarding lot-specific parameters, such as the average operating currents values for the manufacturing lot of claim 17. Rather, to the extent Abrahams discloses that operating parameters are stored in a non-volatile memory, Abrahams discloses the use of general device-specific parameters. For example, Abrahams discloses that "[t]he operational parameters may be *specific to each type of component*." Abrahams, page 2, paragraph 23 (emphasis added). In view of this teach of Abrahams, there is no convincing line of reasoning as to why one of ordinary skill in the art would modify Abrahams in the manner recited in independent claim 17.

Appellants further assert that Nerl fails to remedy the deficiencies of Abrahams. Indeed, the Examiner merely referred to Nerl for its alleged teaching that it is well known in the art that a DIMM can be an FRU. Final Office Action, page 14. Accordingly, even if Nerl disclosed what is asserted by the Examiner, it does not remedy the deficiencies discussed above.

In view of the remarks set forth above, Appellants respectfully submit that independent claim 17 and its dependent claims are not rendered obvious by the cited combination. Accordingly, Appellants request withdrawal of the Examiner's rejection and allowance of claims 17-20.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: February 11, 2008

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8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1. A method of configuring a system comprising:

reading operating current values from a non-volatile memory device on a memory module, wherein the memory module comprises a plurality of volatile memory devices, and wherein the operating current values comprise operating currents uniquely corresponding to a lot in which the volatile memory devices were manufactured; and

configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module.

2. The method, as set forth in claim 1, wherein reading comprises reading operating current values from a serial presence detect device.

3. The method, as set forth in claim 1, wherein reading comprises reading operating current values from a non-volatile memory device on a dual inline memory module.

4. The method, as set forth in claim 1, wherein reading comprises reading the operating current values from the non-volatile memory device during a boot of the system.

5. The method, as set forth in claim 1, wherein configuring comprises setting operating current thresholds in the system in accordance with the operating current values.

6. The method, as set forth in claim 5, comprising throttling the memory module if an actual operating current in the memory module exceeds one of the operating current thresholds.

7. A method of configuring a system comprising:

reading operating current values from a non-volatile memory device on a memory module, wherein the memory module comprises a plurality of volatile memory devices, and wherein the operating current values comprise operating currents uniquely corresponding to each of the plurality of memory devices; and

configuring the system in accordance with the operating current values from the non-volatile memory device on the memory module.

8. The method, as set forth in claim 7, wherein reading comprises reading operating current values from a serial presence detect device.

9. The method, as set forth in claim 7, wherein reading comprises reading operating current values from a non-volatile memory device on a dual inline memory module.

10. The method, as set forth in claim 7, wherein reading comprises reading the operating current values from the non-volatile memory device during a boot of the system.

11. The method, as set forth in claim 7, wherein configuring comprises setting operating current thresholds in the system in accordance with the operating current values.

12. The method, as set forth in claim 11, comprising throttling the memory module if an actual operating current in the memory module exceeds one of the operating current thresholds.

13. A method of manufacturing a memory module comprising:

measuring operating current values in each of a plurality of volatile memory devices;

storing each of the operating current values corresponding to each of the plurality of volatile memory devices in a non-volatile memory device; and

forming a memory module comprising each of the plurality of volatile memory devices and the non-volatile memory device.

14. The method, as set forth in claim 13, wherein measuring comprises measuring the operating current values in each of a plurality of dynamic random access memory devices.

15. The method, as set forth in claim 13, wherein storing comprises storing each of the operating current values corresponding to each of the plurality of volatile memory devices in a serial presence detect device.

16. The method as set forth in claim 13, wherein forming comprises forming a dual inline memory module.

17. A method of manufacturing a memory module comprising:

measuring operating current values in each of a plurality of volatile memory devices, wherein the plurality of volatile memory devices correspond to a single manufacturing lot;

calculating average operating current values for the manufacturing lot;

storing the average operating current values in a non-volatile memory device; and

forming a memory module comprising each of the plurality of volatile memory devices and the non-volatile memory device.

18. The method, as set forth in claim 17, wherein measuring comprises measuring the operating current values in each of a plurality of dynamic random access memory devices.

19. The method, as set forth in claim 17, wherein storing comprises storing the average operating current values in a serial presence detect device.

20. The method as set forth in claim 17, wherein forming comprises forming a dual inline memory module.

21. A memory module comprising:

a plurality of volatile memory devices; and

a non-volatile memory device having operating current values uniquely corresponding to a lot in which the plurality of volatile memory devices were manufactured stored thereon.

22. The memory module, as set forth in claim 21, wherein the memory module comprises a dual inline memory module.

23. The memory module, as set forth in claim 21, wherein each of the plurality of volatile memory devices comprises a dynamic random access memory device.

24. The memory module, as set forth in claim 21, wherein the non-volatile memory device comprises a serial presence detect device.

25. A memory module comprising:

a plurality of volatile memory devices; and

a non-volatile memory device having operating current values uniquely corresponding to each of the plurality of volatile memory devices stored thereon.

26. The memory module, as set forth in claim 25, wherein the memory module comprises a dual inline memory module.

27. The memory module, as set forth in claim 25, wherein each of the plurality of volatile memory devices comprises a dynamic random access memory device.

28. The memory module, as set forth in claim 25, wherein the non-volatile memory device comprises a serial presence detect device.

29. A computer system comprising:

a processor; and

a memory module coupled to the processor and comprising:

a plurality of volatile memory devices; and

a non-volatile memory device having operating current values uniquely corresponding to each of the plurality of volatile memory devices stored thereon.

30. The computer system, as set forth in claim 29, wherein the memory module comprises a dual inline memory module.

31. The computer system, as set forth in claim 29, wherein each of the plurality of volatile memory devices comprises a dynamic random access memory device.

32. The computer system, as set forth in claim 29, wherein the non-volatile memory device comprises a serial presence detect device.

9. **EVIDENCE APPENDIX**

None.

10. <u>RELATED PROCEEDINGS APPENDIX</u>

None.